

# DATA SHEET

## **74AVC16374**

**16-bit edge triggered D-type  
flip-flop; 3.6 V tolerant; 3-state**

Product Specification  
Supersedes data of 1998 Dec 11  
File under Integrated Circuits, IC24

2000 Mar 09

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**74AVC16374**

**FEATURES**

- Wide supply voltage range from 1.2 to 3.6 V
- Complies with JEDEC standard no. 8-1A/5/7
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- DCO (Dynamic Controlled Output) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple  $V_{CC}$  and GND pins to minimize noise and ground bounce
- Supports Live Insertion.

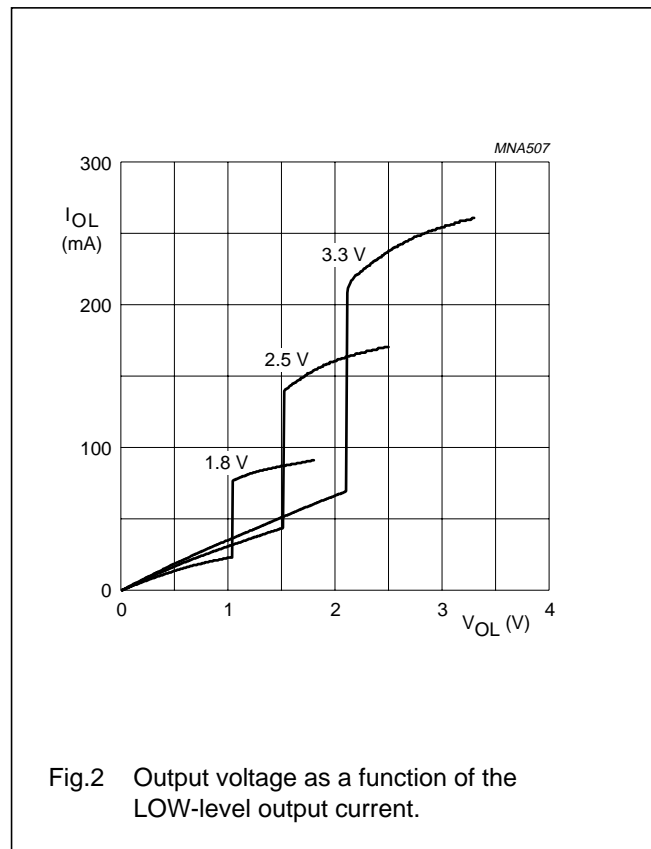
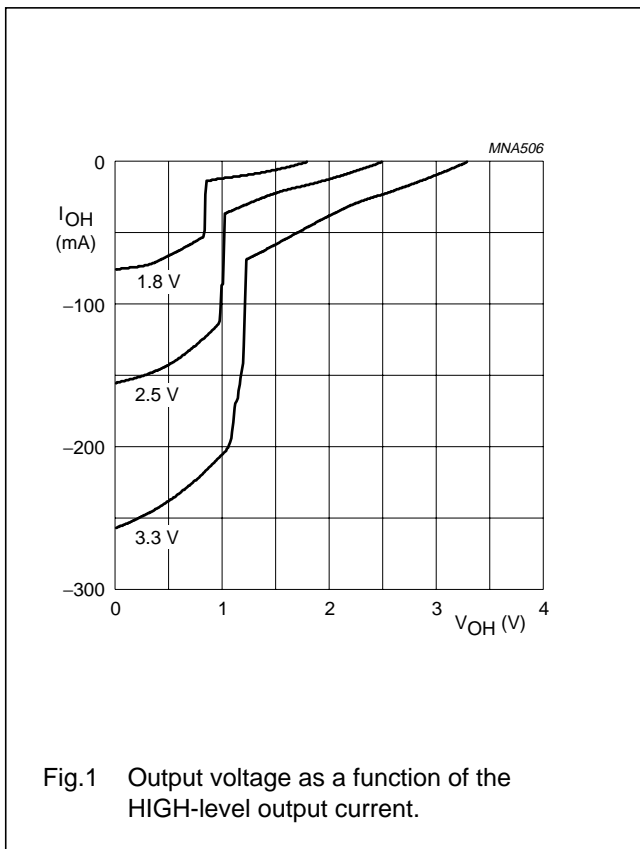
**DESCRIPTION**

The 74AVC16374 is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. The 74AVC16374 consist of 2 sections of eight edge triggered flip-flops. A clock input (CP) and an output enable ( $\overline{OE}$ ) are provided per 8-bit section.

The 74AVC16374 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down,  $n\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see Figs 1 and 2).



# 16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

74AVC16374

**QUICK REFERENCE DATA**GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nCP to nQ <sub>n</sub>	$V_{CC} = 1.2\text{ V}$	3.1	ns
		$V_{CC} = 1.5\text{ V}$	2.4	ns
		$V_{CC} = 1.8\text{ V}$	2.0	ns
		$V_{CC} = 2.5\text{ V}$	1.5	ns
		$V_{CC} = 3.3\text{ V}$	1.3	ns
$f_{max}$	maximum clock pulse frequency	$V_{CC} = 1.2\text{ V}$	250	MHz
		$V_{CC} = 1.5\text{ V}$	300	MHz
		$V_{CC} = 1.8\text{ V}$	320	MHz
		$V_{CC} = 2.5\text{ V}$	350	MHz
		$V_{CC} = 3.3\text{ V}$	350	MHz
$C_i$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per buffer	notes 1 and 2 outputs enabled	66	pF
		outputs disabled	1	pF

**Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. The condition is  $V_i = \text{GND to } V_{CC}$ .

**FUNCTION TABLE**

See note 1.

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	nOE	nCP	nD <sub>n</sub>		nQ <sub>n</sub>
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

**Note**

1. H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 Z = high impedance OFF-state;  
 ↑ = LOW-to-HIGH CP transition.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

**ORDERING AND PACKAGE INFORMATION**

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AVC16374DGG	-40 to +85 °C	48	TSSOP	plastic	SOT362-1

**PINNING**

PIN	SYMBOL	DESCRIPTION
1	1 $\overline{OE}$	output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11 and 12	1Q <sub>0</sub> to 1Q <sub>7</sub>	3-state flip-flop outputs
4, 10, 15, 21, 28, 34, 39 and 45	GND	ground (0 V)
7, 18, 31 and 42	V <sub>CC</sub>	DC supply voltage
13, 14, 16, 17, 19, 20, 22 and 23	2Q <sub>0</sub> to 2Q <sub>7</sub>	3-state flip-flop outputs
24	2 $\overline{OE}$	output enable input (active LOW)
25	2CP	clock input
26, 27, 29, 30, 32, 33, 35 and 36	2D <sub>7</sub> to 2D <sub>0</sub>	data inputs
37, 38, 40, 41, 43, 44, 46 and 47	1D <sub>7</sub> to 1D <sub>0</sub>	data inputs
48	1CP	clock input

16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

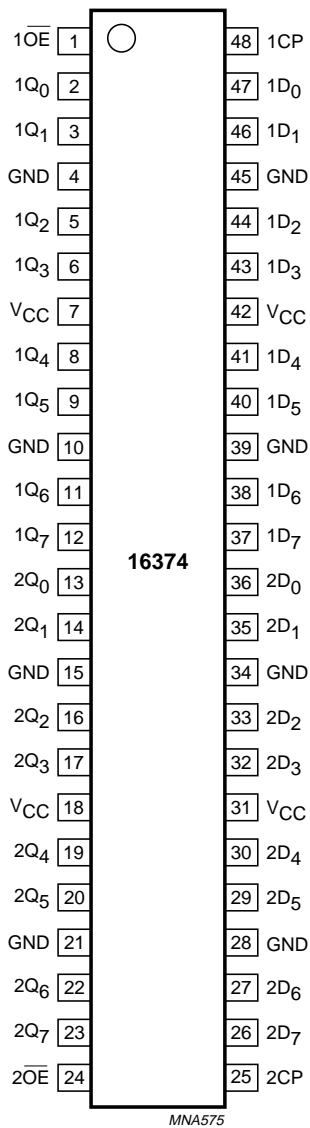


Fig.3 Pin configuration.

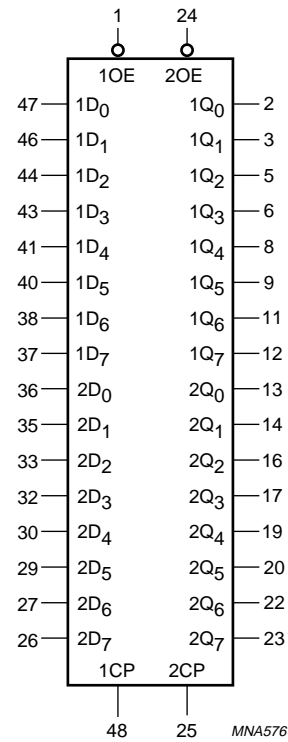


Fig.4 Logic symbol.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

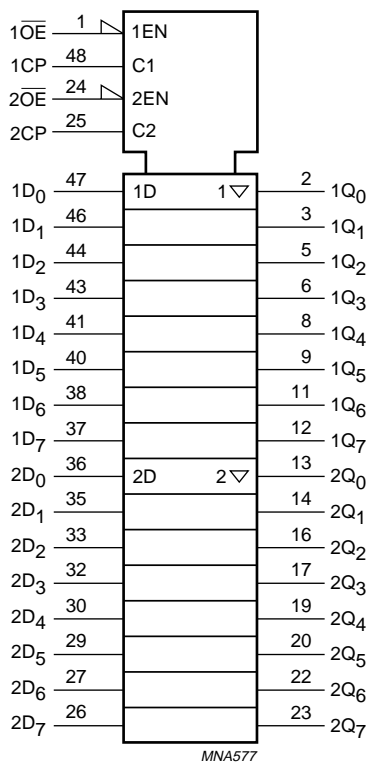


Fig.5 IEEE/IEC logic symbol.

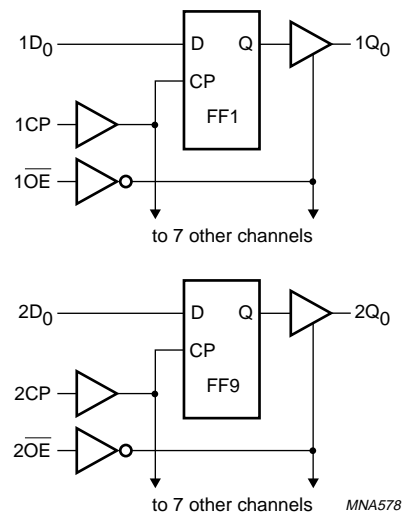


Fig.6 Logic diagram.

# 16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

74AVC16374

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	DC supply voltage	according to JEDEC Low Voltage Standards	1.4	1.6	V
			1.65	1.95	V
			2.3	2.7	V
			3.0	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	DC input voltage		0	3.6	V
V <sub>O</sub>	DC output voltage	output 3-state	0	3.6	V
		output HIGH or LOW state	0	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall time ratios	V <sub>CC</sub> = 1.4 to 1.6 V	0	40	ns/V
		V <sub>CC</sub> = 1.65 to 2.3 V	0	30	ns/V
		V <sub>CC</sub> = 2.3 to 3.0 V	0	20	ns/V
		V <sub>CC</sub> = 3.0 to 3.6 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	DC input voltage	for inputs; note 1	-0.5	+4.6	V
I <sub>OK</sub>	DC output clamping diode current	V <sub>O</sub> < 0	-	-50	mA
V <sub>O</sub>	DC output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 1	-0.5	+4.6	V
I <sub>O</sub>	DC output sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	50	mA
I <sub>CC</sub> , I <sub>GND</sub>	DC V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>D</sub>	power dissipation per package	for temperature range: -40 to +85 °C; note 2	-	500	mW

### Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P<sub>D</sub> derates linearly with 5.5 mW/K.

# 16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

74AVC16374

## DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb} = -40 \text{ to } +85 \text{ } ^\circ\text{C}$			UNIT
		OTHER	$V_{CC}$ (V)	MIN.	TYP. <sup>(1)</sup>	MAX.	
$V_{IH}$	HIGH-level input voltage		1.2	$V_{CC}$	–	–	V
			1.4 to 1.6	$0.65 \times V_{CC}$	0.9	–	V
			1.65 to 1.95	$0.65 \times V_{CC}$	0.9	–	V
			2.3 to 2.7	1.7	1.2	–	V
			3.0 to 3.6	2.0	1.5	–	V
$V_{IL}$	LOW-level input voltage		1.2	–	–	GND	V
			1.4 to 1.6	–	0.9	$0.35 \times V_{CC}$	V
			1.65 to 1.95	–	0.9	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	1.2	0.7	V
			3.0 to 3.6	–	1.5	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ $I_O = -100 \mu\text{A}$	1.65 to 3.6	$V_{CC} - 0.20$	$V_{CC}$	–	V
		$I_O = -3 \text{ mA}$	1.4	$V_{CC} - 0.35$	$V_{CC} - 0.23$	–	V
		$I_O = -4 \text{ mA}$	1.65	$V_{CC} - 0.45$	$V_{CC} - 0.25$	–	V
		$I_O = -8 \text{ mA}$	2.3	$V_{CC} - 0.55$	$V_{CC} - 0.38$	–	V
		$I_O = -12 \text{ mA}$	3.0	$V_{CC} - 0.70$	$V_{CC} - 0.48$	–	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ $I_O = 100 \mu\text{A}$	1.65 to 3.6	–	GND	0.20	V
		$I_O = 3 \text{ mA}$	1.4	–	0.10	0.35	V
		$I_O = 4 \text{ mA}$	1.65	–	0.10	0.45	V
		$I_O = 8 \text{ mA}$	2.3	–	0.26	0.55	V
		$I_O = 12 \text{ mA}$	3.0	–	0.36	0.70	V
$I_I$	input leakage current per pin	$V_I = V_{CC}$ or GND	1.4 to 3.6	–	0.1	2.5	$\mu\text{A}$
$I_{off}$	power-off leakage current	$V_I$ or $V_O = 3.6 \text{ V}$	0	–	0.1	$\pm 10$	$\mu\text{A}$
$I_{IHZ}/I_{ILZ}$	input current for common I/O pins	$V_I = V_{CC}$ or GND	1.4 to 3.6	–	0.1	12.5	$\mu\text{A}$
$I_{OZ}$	3-state output OFF-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	1.4 to 2.7	–	0.1	5	$\mu\text{A}$
			3.0 to 3.6	–	0.1	10	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	1.4 to 2.7	–	0.1	20	$\mu\text{A}$
			3.0 to 3.6	–	0.2	40	$\mu\text{A}$

### Note

1. All typical values are measured at  $T_{amb} = 25 \text{ } ^\circ\text{C}$ .



**16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state**

74AVC16374

**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.0$  ns.

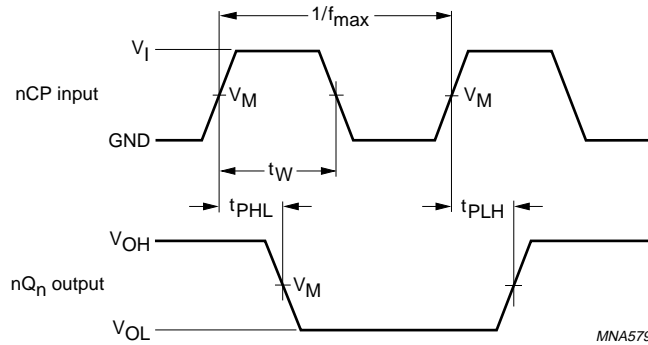
SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb} = -40$ to $+85$ °C			UNIT
		WAVEFORMS	$V_{CC}$ (V)	MIN.	TYP. <sup>(1)</sup>	MAX.	
$t_{PHL}/t_{PLH}$	propagation delay nCP to nQ <sub>n</sub>	see Figs 7 and 10	1.2	–	3.1	–	ns
			1.40 to 1.60	1.2	2.4	8.4	ns
			1.65 to 1.95	1.0	2.0	6.7	ns
			2.3 to 2.7	0.8	1.5	4.1	ns
			3.0 to 3.6	0.7	1.3	3.3	ns
$t_{PZH}/t_{PZL}$	3-state output enable time nOE to nQ <sub>n</sub>	see Figs 8 and 10	1.2	–	5.4	–	ns
			1.40 to 1.60	1.6	3.9	8.5	ns
			1.65 to 1.95	2.3	3.3	6.7	ns
			2.3 to 2.7	0.9	2.3	4.3	ns
			3.0 to 3.6	0.7	2.0	3.4	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time nOE to nQ <sub>n</sub>	see Figs 8 and 10	1.2	–	5.6	–	ns
			1.40 to 1.60	2.5	4.5	9.4	ns
			1.65 to 1.95	1.8	3.3	7.8	ns
			2.3 to 2.7	1.0	1.8	4.2	ns
			3.0 to 3.6	1.2	2.0	3.9	ns
$t_w$	nCP pulse width HIGH	see Figs 7 and 10	1.2	–	0.8	–	ns
			1.40 to 1.60	–	0.5	–	ns
			1.65 to 1.95	3.1	0.3	–	ns
			2.3 to 2.7	2.5	0.2	–	ns
			3.0 to 3.6	2.5	0.2	–	ns
$t_{su}$	set-up time nD <sub>n</sub> to nCP	see Figs 9 and 10	1.2	–	–0.6	–	ns
			1.40 to 1.60	2.7	–0.3	–	ns
			1.65 to 1.95	1.9	–0.3	–	ns
			2.3 to 2.7	1.4	–0.2	–	ns
			3.0 to 3.6	1.4	–0.1	–	ns
$t_h$	hold time nD <sub>n</sub> to nCP	see Figs 9 and 10	1.2	–	0.8	–	ns
			1.40 to 1.60	1.3	0.7	–	ns
			1.65 to 1.95	1.2	0.6	–	ns
			2.3 to 2.7	1.1	0.5	–	ns
			3.0 to 3.6	1.1	0.4	–	ns
$f_{max}$	maximum clock pulse frequency	see Figs 7 and 10	1.2	–	250	–	MHz
			1.40 to 1.60	–	300	–	MHz
			1.65 to 1.95	160	320	–	MHz
			2.3 to 2.7	200	350	–	MHz
			3.0 to 3.6	200	350	–	MHz

**Note**1. All typical values are measured at  $T_{amb} = 25$  °C and at  $V_{CC}$  respectively 1.2, 1.5, 1.8, 2.5 and 3.3 V.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

AC WAVEFORMS

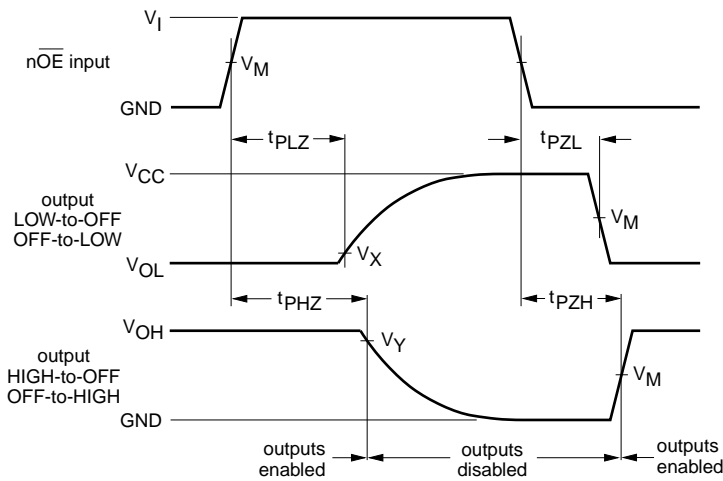


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V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
≤2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
3.0 to 3.6 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 Clock input (nCP) to output (nQ<sub>n</sub>) propagation delays.



MNA478

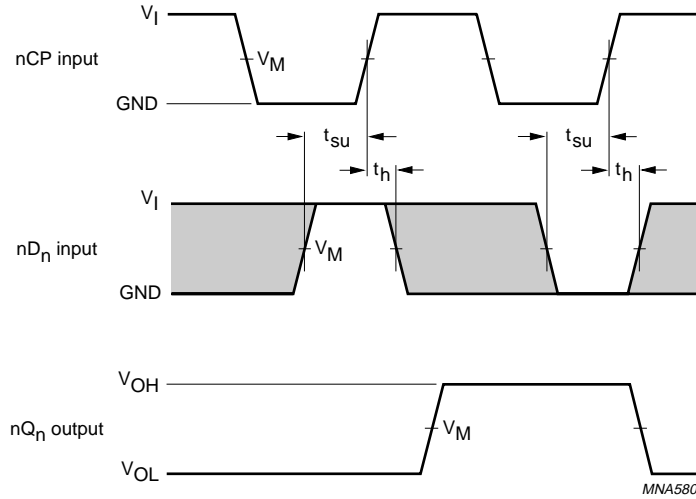
V <sub>CC</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>	V <sub>I</sub>
≤2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V	V <sub>CC</sub>
3.0 to 3.6 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V	V <sub>CC</sub>

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.8 3-state enable and disable times.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

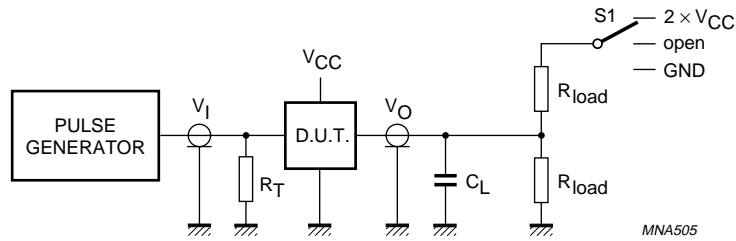


The shaded areas indicate when the input is permitted to change for predictable output performance.

V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
≤2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
3.0 to 3.6 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.9 Data set-up and hold times for nD<sub>n</sub> input to nCP input.



TEST	S1	V <sub>CC</sub> (V)	V <sub>I</sub>	R <sub>load</sub>	C <sub>L</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	open	1.2	V <sub>CC</sub>	2000 Ω	15 pF
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>	1.4 – 1.6	V <sub>CC</sub>	2000 Ω	15 pF
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND	1.65 – 1.95	V <sub>CC</sub>	1000 Ω	30 pF
		2.3 – 2.7	V <sub>CC</sub>	500 Ω	30 pF
		3.0 – 3.6	V <sub>CC</sub>	500 Ω	30 pF

Fig.10 Load circuitry for switching times.

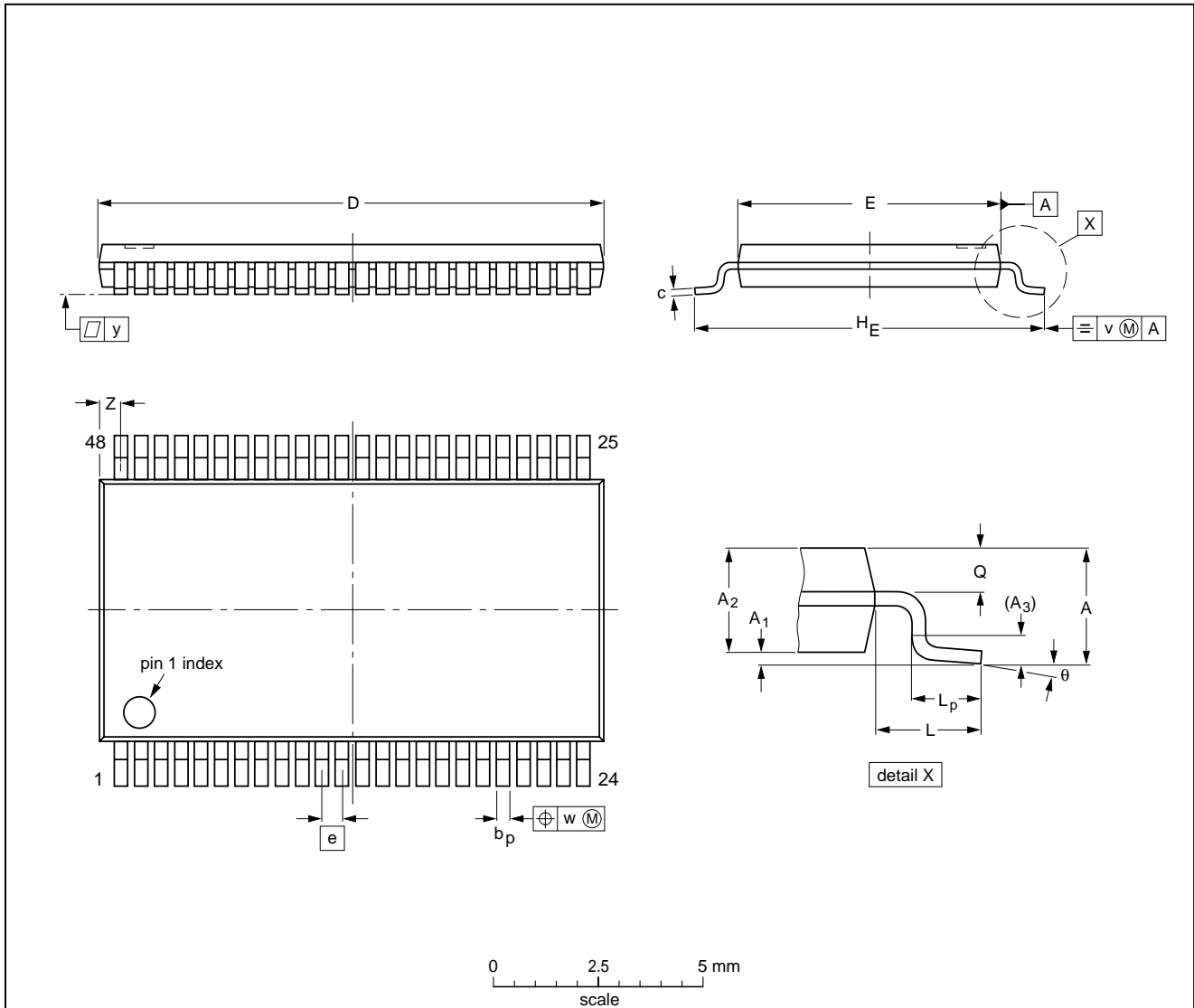
16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

PACKAGE OUTLINE

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				95-02-10 99-12-27

## 16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

74AVC16374

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

74AVC16374

#### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

#### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

#### DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

#### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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16-bit edge triggered D-type flip-flop; 3.6 V tolerant;  
3-state

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74AVC16374

**NOTES**

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SCA 69

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